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PCI-SIG ENGINEERING CHANGE REQUEST

1. PCI-SIG ENGINEERING CHANGE NOTICE

TITLE:	NCTF Ground Ball Definition for PCIe BGA SSD 11.5x13
DATE:	December 13, 2017
AFFECTED DOCUMENT:	PCIe BGA SSD 11.5x13 ECR
SPONSOR:	Intel, Western Digital

Part I

1.1. Summary of the Functional Changes

This proposal redefines the outer most ring of ground pins in the 11.5x13 BGA ball map to be redundant ground pins that are non-critical to function (NCTF).

NCTF is a new pin definition indicating that while the pins shall continue to be connected to host and device ground, they are redundant such that they allow for mechanical failure but not functional failure.

1.2. Benefits as a Result of the Changes

The outer ring in of balls in the 11.5 mm x13 mm ballmap was added with the intent that it would provide thermal and structural benefit only. This change eases electrical performance qualification without reducing or minimizing package reliability.

1.3. Assessment of the Impact

This change has no impact on the 11.5 mm x 13 mm form factor or any of the other BGA form factors. The change does require updates to signal definitions and parameters throughout Section 3.4: “BGA SSD Interface Signals”, relevant to the new NCTF pin definition for redundant ground. 1113 pinouts in Section 3.4 and Section 5 require updates as well.

1.4. Analysis of the Hardware Implications

Naming impact only for outer most ring of ground pins, changing to be defined as NCTF. No physical connectivity impact of change.

1.5. Analysis of the Software Implications

N/A.

1.6. Analysis of the C&I Test Implications

N/A.

[Editor's note: Existing M.2 v1.1 text is black. New text is marked in blue with underscore. Material to be deleted ~~is red with strikethrough~~.]

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3.4 BGA SSD Interface Signals

Table 39a contains a list of the signals defined for BGA SSDs. The I/O direction indicated is from BGA module's perspective.

Table 39a. BGA SSD System Interface Signal Table for Type 1113

Interface	Signal Name	I/O	Function	Voltage
Power and Grounds	PWR_1 (10 pins)	I	+3.3 V supply	
	PWR_2 (20 pins)	I	+1.2 V or +1.8 V supply	
	PWR_3 (10 pins)	I	+0.9 V, +1.1 V, or +1.2 V supply	
	GND (~~115~~75 pins)		Return current path	
	NCTF (40 pins)		Non Critical To Function pins. Redundant ground that shall be electrically connected to the common host and device ground plane allowing for mechanical failure but not functional failure.	
PCIe	PERp0, PERn0/ PETp0, PETn0 PERp1, PERn1/ PETp1, PETn1	I/O	PCIe TX/RX Differential signals defined by the *PCI Express Card Electromechanical Specification.*	
	REFCLKp/ REFCLKn	I	PCIe Reference Clock signals (100 MHz) defined by the *PCI Express Card Electromechanical Specification.* **Note**: This reference clock is the common ref clock that shall be used with PCIe.	
	PERST#	I	PE-Reset is a functional reset to the card as defined by the *PCI Express Mini Card Electromechanical Specification*.	1.8 V
	CLKREQ#	I/O	Clock Request is a reference clock request signal as defined by the *PCI Express Mini Card Electromechanical Specification*; also used by L1 PM Substates.	1.8 V

Interface	Signal Name	I/O	Function	Voltage
	PEWAKE#/OBFF	I/O	PCIe WAKE#. Open Drain with pull up on platform. Active Low when used as PEWAKE#. When the add-in module supports wakeup, this signal is used to request that the system return from a sleep/suspend state to service a function initiated wake event. When the add-in module supports OBFF mechanism, the signal is used by the system to indicate OBFF or CPU Active State transitions.	1.8 V
SSD Specific Signals	SUSCLK	I	32.768 kHz clock supply input provided by the platform chipset to reduce power and cost for the module. SUSCLK has a duty cycle that is able to be as low as 30% or as high as 70%. The tolerance for this clock is ±100 ppm.	1.8 V
	LED_1#	O	Open drain, active low signal. This signal is used to allow the Adapter to provide status indication via LED device that will be provided by the system.	3.3 V
	RFU		Reserved for future use.	
	DNU		Do not use. Manufacturing purpose only.	
	HSB		Host specific balls.	
SSD Specific Optional Signals	XTAL_IN	I	Connection to crystal unit.	N/A
	XTAL_OUT	O	Connection to crystal unit.	N/A
	CAL_P	N/A	PCIe PHY calibration resistor.	N/A
	RZQ_1, RZQ_2	N/A	Memory or NAND calibration resistor.	N/A
	JTAG_TRST#	I	Refer to JTAG *Specification (IEEE 1149.1), Test Access Port and Boundary Scan Architecture* for definition of these balls.	3.3 V
	JTAG_TCK	I		
	JTAG_TMS	I		
	JTAG_TDI	I		
	JTAG_TDO	O		
	SMB_CLK	I/O	SMBus Clock, Open Drain with pull up on platform.	1.8 V
	SMB_DATA	I/O	SMBus Data, Open Drain with pull up on platform.	1.8 V
	ALERT#	O	Alert notification to master; Open Drain with pull up on platform; Active Low.	1.8 V
	DIAG0, DIAG1	I/O	Engineering test mode balls have been specified to allow for special access to DIAG for debug purposes.	
	WP_L	I	Write protect signal to prevent writes from occurring to SPI NOR. Active low.	1.8 V
	SPI_CLK	I	SPI clock. Max frequency is 50 MHz.	1.8 V
	SPI_MOSI	I	Master Out Slave In signal for SPI NOR.	1.8 V
	SPI_MISO	O	Master In Slave Out signal for SPI NOR	1.8 V

Interface	Signal Name	I/O	Function	Voltage
	SPI_CS_L	I	Chip select for SPI NOR. Active low.	1.8 V
	SPI_18	I	+1.8 V supply. Optional voltage supply if SPI NOR included in package.	1.8 V
	REG_01	N/A	Connection to internal power rail. Value and usage is vendor specific.	N/A
	REG_02	N/A	Connection to internal power rail. Value and usage is vendor specific.	N/A
	REG_03	N/A	Connection to internal power rail. Value and usage is vendor specific.	N/A

3.4.4. SSD Specific Signals

3.4.4.1. SUSCLK

Definition for this signal is the same as that in section 3.1.12.1 in this specification, except that this signal is defined to be at signal levels of 1.8 V.

3.4.4.2. PEDET

The interface detect can be used by the host computer to determine the communication protocol that the M.2 module uses; SATA signaling (low) or PCIe signaling (high) in conjunction with a platform located pull-up resistor.

Note: This signal is not applicable to Type 1113, which supports only the PCIe interface.

3.4.4.3. Status Indicator (LED_1#)

See section 3.1.12.2, Status Indicators, for a more detailed description of the LED_1# signal.

3.4.4.4. RFU

Signals documented as RFU are reserved for future use. These balls must be soldered to a Platform board, but must be electrically no-connect on the Host ~~or~~ and the Adapter. These balls are reserved for future assignment as a functional signal.

3.4.4.5. DNU (Do Not Use)

Signals documented as DNU are for manufacturing only. These balls must be soldered to a platform, but must be electrically no-connect on the host. Signals documented as DNU are for manufacturing only.

3.4.4.6. HSB (Host Specific Balls)

Signals documented as HSB are not defined as a functional signal. These balls must be soldered to a platform, but must be electrically no-connect on the adapter. A host's use of this signal is undefined.

3.4.4.7. NCTF (Non Critical To Function)

Signals documented as NCTF are redundant ground balls. They are connected to host ground and redundant to other device grounds, so the loss of the solder joint continuity due to mechanical failure at end of life conditions will not affect the overall product functionality.

3.4.6. BGA SSD Soldered-Down Module Pin-out

All pinout tables in this section are written from the module point of view when referencing signal directions.

Figure 105a shows the Type 1113 BGA ballmap (Top View).

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	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	NCTF	NCTF	NCTF			NCTF			NCTF			NCTF			NCTF			NCTF	NCTF	NCTF
B	NCTF	GND	GND	REG_01	REG_02	REG_03			GND			GND			GND	WP_L	SPI_CLK	SPI_CS_L	GND	NCTF
C	NCTF	GND	GND	DNU	DNU	RFU	RFU	RFU	RFU	RFU	SMB_DATA	ALERT#	DIAG0	JTAG_TMS	JTAG_TDI	SPI_MOSI	SPI_MISO	GND	GND	NCTF
D		PWR_2	PWR_2	DNU	DNU	RFU	RFU	RFU	RFU	RFU	SMB_CLK	DIAG1	JTAG_TRST#	JTAG_TDO	JTAG_TCK	RFU	SPI_18	PWR_2	PWR_2	
E	NCTF	PWR_2	PWR_2	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	NCTF
F		PWR_2	PWR_2	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	
G		GND	GND	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	GND	
H	NCTF	PWR_1	PWR_1	HSB	HSB	HSB	HSB								HSB	HSB	GND	PWR_1	PWR_1	NCTF
J		PWR_1	PWR_1	GND	HSB	HSB		HSB	HSB	HSB	HSB	HSB	HSB		HSB	HSB	HSB	PWR_1	PWR_1	
K		GND	PWR_1	HSB	HSB	HSB		HSB					HSB		HSB	HSB	GND	PWR_1	GND	
L	NCTF	RZQ_1	GND	GND	HSB	HSB		HSB					HSB		HSB	HSB	HSB	GND	RZQ_2	NCTF
M	NCTF	GND	PWR_3	HSB	HSB	HSB		HSB					HSB		HSB	HSB	GND	PWR_3	GND	NCTF
N		PWR_3	PWR_3	GND	HSB	HSB		HSB					HSB		HSB	HSB	HSB	PWR_3	PWR_3	
P		PWR_3	PWR_3	HSB	HSB	HSB		HSB	HSB	HSB	HSB	HSB	HSB		HSB	HSB	GND	PWR_3	PWR_3	
R	NCTF	GND	GND	GND	HSB	HSB									HSB	HSB	HSB	GND	GND	NCTF
T		PWR_2	PWR_2	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	
U		PWR_2	PWR_2	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	
V	NCTF	GND	GND	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	GND	GND	NCTF
W		SUSCLK	CLKREQ#	PERST#	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	RFU	CAL_P	XTAL_OUT	XTAL_IN	
Y	NCTF	LED_1#	GND	GND	GND	GND	PERp0	PERn0	GND	PETp0	PETn0	GND	PERp1	PERn1	GND	GND	GND	GND	PEWAKE#	NCTF
AA	NCTF	GND	GND	REFCLKp	REFCLKn	GND			GND			GND			GND	PETp1	PETn1	GND	GND	NCTF
AB	NCTF	NCTF	NCTF			NCTF			NCTF			NCTF			NCTF			NCTF	NCTF	NCTF

Figure 105a. Type 1113 Module-side BGA Ballmap (Top View)

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5. Platform Socket Pinout and Key Definitions

All pinouts tables in this section are written from the platform/system point of view when referencing signal directions.

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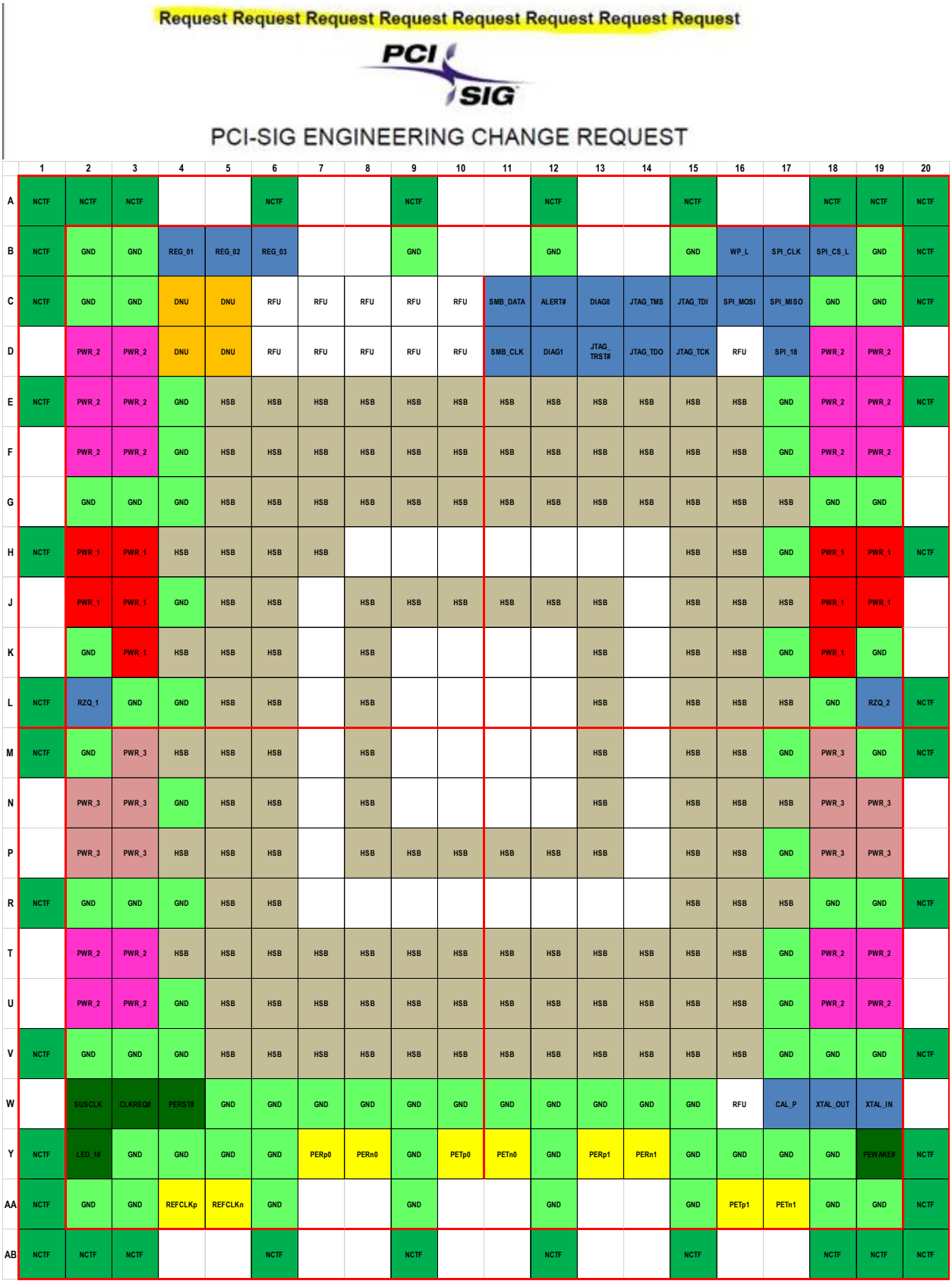
5.4. Soldered Down Pinouts Definitions

The soldered-down pinouts definitions are shown in the following figures:

- Figure 113, *Type 1113 BGA Socket Map On Platform (Top View)*



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	NCTF	NCTF	NCTF			NCTF			NCTF			NCTF			NCTF			NCTF	NCTF	NCTF
B	NCTF	GND	GND	REG_01	REG_02	REG_03			GND			GND			GND	WP_L	SPI_CLK	SPI_CS_L	GND	NCTF
C	NCTF	GND	GND	DNU	DNU	RFU	RFU	RFU	RFU	RFU	SMB_DATA	ALERT#	DIAG0	JTAG_TMS	JTAG_TDI	SPI_MOSI	SPI_MISO	GND	GND	NCTF
D		PWR_2	PWR_2	DNU	DNU	RFU	RFU	RFU	RFU	RFU	SMB_CLK	DIAG1	JTAG_TRST#	JTAG_TDO	JTAG_TCK	RFU	SPI_18	PWR_2	PWR_2	
E	NCTF	PWR_2	PWR_2	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	NCTF
F		PWR_2	PWR_2	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	
G		GND	GND	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	GND	
H	NCTF	PWR_1	PWR_1	HSB	HSB	HSB	HSB								HSB	HSB	GND	PWR_1	PWR_1	NCTF
J		PWR_1	PWR_1	GND	HSB	HSB		HSB	HSB	HSB	HSB	HSB	HSB		HSB	HSB	HSB	PWR_1	PWR_1	
K		GND	PWR_1	HSB	HSB	HSB		HSB					HSB		HSB	HSB	GND	PWR_1	GND	
L	NCTF	RZQ_1	GND	GND	HSB	HSB		HSB					HSB		HSB	HSB	HSB	GND	RZQ_2	NCTF
M	NCTF	GND	PWR_3	HSB	HSB	HSB		HSB					HSB		HSB	HSB	GND	PWR_3	GND	NCTF
N		PWR_3	PWR_3	GND	HSB	HSB		HSB					HSB		HSB	HSB	HSB	PWR_3	PWR_3	
P		PWR_3	PWR_3	HSB	HSB	HSB		HSB	HSB	HSB	HSB	HSB	HSB		HSB	HSB	GND	PWR_3	PWR_3	
R	NCTF	GND	GND	GND	HSB	HSB									HSB	HSB	HSB	GND	GND	NCTF
T		PWR_2	PWR_2	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	
U		PWR_2	PWR_2	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	
V	NCTF	GND	GND	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	GND	GND	NCTF
W		SUSCLK	CLKREQ#	PERST#	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	RFU	CAL_P	XTAL_OUT	XTAL_IN	
Y	NCTF	LED_1#	GND	GND	GND	GND	PERp0	PERn0	GND	PETp0	PETn0	GND	PERp1	PERn1	GND	GND	GND	GND	PEWAKE#	NCTF
AA	NCTF	GND	GND	REFCLKp	REFCLKn	GND			GND			GND			GND	PETp1	PETn1	GND	GND	NCTF
AB	NCTF	NCTF	NCTF			NCTF			NCTF			NCTF			NCTF			NCTF	NCTF	NCTF

Figure 113. Type 1113 BGA Socket Map On Platform (Top View)

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6. Annex

6.1. Glossary

A	Amperage or Amp	**NCTF**	Non Critical To Function
BGA	Ball Grid Array	**NIC**	Network Interface Card
BIOS	Basic Input Output System	**N/C**	Not Connected
BTO	Build-to-Order	**OD**	Open Drain
CEM	Card Electromechanical	**OEM**	Original Equipment Manufacturer
CTO	Configure To Order	**OS**	Operating System
DC	Direct Current	**PCIe**	Peripheral Component Interconnect Express
DNU	Do Not Use	**SATA**	Serial Advanced Technology Attachment or Serial ATA
DPR	Dynamic Power Reduction	**PCM**	Pulse Code Modulation
GND	Ground	**RF**	Radio Frequency
GNSS	Global Navigation Satellite System (GPS+GLONASS)	**RFU**	Reserved for Future Use
HDR	Hybrid Digital Radio	**RMS**	Root Mean Square
HSIC	High Speed Inter-Chip	**RoHS**	Restriction of Hazardous Substances Directive
I/F	Interface	**RSS**	Root Sum Square
I/O (O/I)	Input/Output (Output/Input)	**RTC**	Real Time Clock
IR	Current x Resistance = Voltage	**SDIO**	Secure Digital Input Output
I^2C	Inter-Integrated Circuit	**SIM**	Subscriber Identity Module
I2S	Integrated Interchip Sound	**SSD**	Sold-State Drive
LED	Light Emitting Diode	**SSIC**	Super Speed USB Inter-Chip
LGA	Land Grid Array	**RF**	Radio Frequency
M-PCIe	Mobile PCIe	**USB**	Universal Serial Bus
mΩ	milli Ohm	**UART**	Universal Asynchronous Receive Transmit
mA	milli Amp	**V**	Voltage
mm	milli meter	**W**	Wattage or Watts
mV	milli Volt	**WiGig**	60 GHz multi-gigabit speed wireless communication
NFC	Near Field Communications	**WLAN**	Wireless Local Area Network
M.2	Formerally called Next Generation Form Factor (NGFF)	**WPAN**	Wireless Personal Area Network
NB	Notebook	**WWAN**	Wireless Wide Area Network